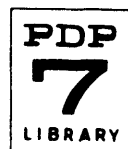


- 1. IDENTIFICATION
- 1.1 MAINDEC 703
- 1.2 PDP-7 Memory Address Test
- 1.3 July 7, 1965



2. ABSTRACT

The Memory Address Test is designed to provide a rough inspection of the performance of the memory address register and the decoder networks which select a given cell. Maindec 703 will operate in and test memories of any available capacity from 4096 to 32,768 words.

3. REQUIREMENTS

3.1 Storage

The program occupies memory registers 00000-00022, in memory field 0. In addition, a short initializing sequence which determines the size of the memory occupies registers 00023-00044; this sequence is destroyed once the test begins.

3.2 Subprograms

None.

3.3 Equipment

Standard PDP-7 with or without memory extension control and up to three extended memory fields.

4. USAGE

4.1 Loading

4.1.1 Place the HRI program tape in the reader.

4.1.2 Set the address switches to 00000.

4.1.3 Clear the AC switches, then set ACS_{3-4} to indicate the number of additional memory fields provided, according to the following table:

<u>No. of Added Fields</u>	<u>Total Memory Size</u>	<u>ACS_3</u>	<u>ACS_4</u>
0	4K, 8K	0	0
1	12K, 16K	0	1
2	20K, 24K	1	0
3	28K, 32K	1	1

4.1.4 Press READ-IN

The program will start automatically.

4.2 Calling Sequence (Not Applicable)

4.3 Switch Settings

4.3.1 Loading Address

00000

4.3.2 Restart Address

00001

4.3.3 Other Settings

AC Switches 3, 4: Number of extended memory fields
Restart: EXTEND switch on

4.4 Startup

The program starts automatically after being loaded. To restart the program at any time afterwards, set the address switches to 00001, turn on the EXTEND switch and press START.

4.5 Errors

The following error stops appear in succession for each error.

ERROR: E1
C(MA): 00014
C(AC): Failed bits as 1's

XOR → The contents of the memory cell just examined were incorrect. The AC lights display the results of a comparison between the contents of the register and the address of that register. Bits which did not match are shown as 1's in a field of 0's.

ERROR: E1A
C(MA): 00016
C(AC): Address of failed cell

This halt occurs immediately after E1. The AC lights display the address of the cell causing the error.

4.6 Recovery from such errors

ERROR: E1
RECOVERY: Record the C(AC). Press CONTINUE.

ERROR: E1A
RECOVERY: Record the C(AC). Press CONTINUE.

*unless first pass,
when START at 1 is
required*

5. RESTRICTIONS

When restarting the program without reloading it, the EXTEND switch must be on.

6. DESCRIPTION

6.1 Discussion

Maindec 703 tests each register in sequence, from the low end of the testable area to the highest location, then repeats from the beginning. It continues until an error occurs or until the operator stops the computer.

Before the test begins, an initializing routine determines the size of the core memory in which the test is operating, and accordingly adjusts a constant which sets the upper limit of the testable area. The number of additional memory fields is obtained from the ACS; the size of the last field (4K or 8K) is then established, and the limiting constant is adjusted. The initializing sequence is destroyed when the test begins, so that as much of the memory as possible is available for testing.

The test passes occur in pairs. During the first, the program deposits in a memory cell a quantity equal in value to the quantity of that cell. If the deposit and read operations were successful, the program continues to the next register in sequence. When all of the testable area has been checked by this "write-then-read" procedure, the program goes back to the beginning of that area and attempts to read the contents of each cell. If this "read-only" pass is successful, the program begins a new "write-then-read" cycle. The test continues to alternate the two passes.

When an error occurs during a "write-then-read" pass, the writing is suppressed for the remainder of that pass, to insure that errors further along are not obliterated.

6.2 Applications

In general, the address test will catch two kinds of difficulty in the selection networks. If a selection line is open at any point, the memory registers selectable by that line are, in effect, isolated from the central processor. The program will be unable to write information into those cells or read information out from them. On the other hand, if two selection lines are shorted together, information entering or leaving the registers selectable by one line will also enter or leave those selectable by the other. In this case, the same information will appear in two different memory cells.

A single address selection failure is not likely to occur by itself. Usually there will be a pattern of errors appearing throughout the tested portion of memory, which will allow the operator to isolate the possible sources of trouble. The pattern is most often that of alternating blocks of erroneous and error-free registers.

The following rule of thumb will help the operator track down failing selection lines: If errors occur in blocks of 100_8 registers or more, the trouble lies in the y-axis selection lines. If errors occur in blocks of 77_8 registers or fewer, the trouble lies in the x-axis lines.

Normally, Maindec 703 will test all of available memory, from register 23 to the upper limit. There are two ways to restrict the test area. The upper limit can be lowered to exclude one or more memory fields by setting ACS₃₋₄ accordingly when the program is read in. For example, if a PDP-7 has two additional fields for a total memory capacity of 24,576 words, the operator can test only the lower two fields by setting ACS₃₋₄ to 1, thus limiting the test area to the first 16,384 words.

The lower limit can be changed by manually depositing in register 21 a number one less than the lowest address to be tested. For example, to test only the uppermost memory field on a machine equipped with 24,576 words, place the quantity 57777 in register 00021. This register, labeled LOWT in the program listing, normally contains the number 00021.

Maindec 703 is useful as a rough check of the memory selection networks when performing routine maintenance tests. It can also be used to confirm an operator's suspicions if trouble appears during the normal use of the computer. Sometimes the difficulty can be corrected by the replacement of a module; usually, however, troubles arising from failures in the address selection and memory read-write circuits are likely to require the attention of a field service engineer.

7. METHODS

See Discussion, Section 6.1

8. FORMAT (Not Applicable)

9. EXECUTION TIME

The program runs continuously, taking about 75 msec for each 4096 words of memory, until an error occurs, or until the operator stops the computer. The following table gives the time required for one pass for each possible memory size.

<u>Memory Size</u>	<u>Time (Approximately)</u>	<u>Memory Size</u>	<u>Time (Approximately)</u>
4K	75 msec	20K	375 msec
8K	150 msec	24K	450 msec
12K	225 msec	28K	525 msec
16K	300 msec	32K	600 msec

10. PROGRAM

10.4 Program Listings

10. PROGRAM

10.4 Program Listing

MAINDEC 703: PDP-7 ADDRESS TEST

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0/ /TESTS 22-TOP INCLUDING EXTENSIONS.

ENTR, CML /START NEW PASS HERE
      LAC LOWT /INITIALIZE ADDRESS
      DAC LOX

NEXT, ISZ LOX /MAIN LOOP
      LAC LOX
      SAD TOP /END OF MEMORY?
      JMP ENTR-1 /YES
      SNL /NO. WRITING THIS PASS?
      DAC I LOX /YES.
      XOR I LOX /COMPARISON TEST.
      SNA /C(LOX)=C(I LOX)?
      JMP NEXT /YES, IF C(AC)=0

EI, HLT /ERROR: AC SHOWS WRONG BITS AS 1'S
EIA, LAC LOX
      HLTISTL /AC SHOWS ADDRESS
      JMP NEXT

TOP, 0 /MEMORY LIMIT
LOWT, . /LOWER TEST LIMIT
LOX, 0 /LOCATION INDEX

GO, CAF /MEMORY SIZER
     CLOF
     LASICLL /NO. OF FIELDS FROM AC
     XOR HALF
     DAC HALF /TEST ADDRESS IN LOWER 4K
     XOR FULL
     DAC LOX /TEST ADDRESS IN UPPER 4K
     EEM
     DZM I HALF /CLEARS LOC. 7777 IN HIGHEST FIELD
     DAC I LOX /PUTS AC IN 17777 IN SAME FIELD
     SAD I HALF /ARE THE TWO CELLS DIFFERENT?
     XOR FULL /NO. MASK OUT 8K BIT.
     ADD ONE /TO FORM LIMITING ADDRESS
     DAC TOP
     JMP ENTR

HALF, 7777
FULL, 10000
ONE, 1
EEM=707702
PAUSE GO

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MAINDEC 703 PDP-7 ADDRESS TEST

EEM	707702
ENTR	1
E1	14
E1A	16
FULL	43
GO	23
HALF	42
LOWT	21
LOX	22
NEXT	3
ONE	44
TOP	20

ENTR	1
NEXT	3
E1	14
E1A	16
TOP	20
LOWT	21
LOX	22
GO	23
HALF	42
FULL	43
ONE	44
EEM	707702

11. DIAGRAMS

11.1 Flow Chart

